A Rectifying Circuit With High-Efficiency DC and Harmonic Generations

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***Abstract*—Rectifying circuits are key components in wireless energy harvesting (WEH) systems. In this brief, we propose a new circuit configuration that features simultaneous high-efficiency direct-current (DC) and second-harmonic (SH) generations. Based on a conventional single-series Schottky diode-based rectifying circuit, a bandpass filter is created and innovatively connected to the anode of the diode, which serves as an effective route to output the SH component produced by the diode, yet without sacrificing the DC generation. A prototype is fabricated and measured. The results show that when the input fundamental-frequency power is 19 dBm, the DC conversion efficiency is 55.0%; more importantly, the SH power reaches 9.8 mW, corresponding to a distinctive conversion efficiency of 12.3%. This is higher than previous works without using amplifiers or other active facilities, leading to a competitive overall efficiency of 67.3%. The enhancement of SH is of great significance in improving readout distance and communication quality if it is utilized as an echo signal in backscattering communications. Therefore, this simple and low-cost circuit can find potential applications in WEH and battery-free backscattering systems.**

***Index Terms*—Bandpass filter, high efficiency, rectifying circuit, Schottky diode, second harmonic.**

I. Introduction

SINCE the last century, the concept of wireless power transfer (WPT) has been proposed and the development has been fueled by the advances in microwaves and low-power electronics. It is widely believed that electromagnetic (EM)-based WPT and wireless energy harvesting (WEH) technologies can be the promising recipe to energize wireless apparatuses, extending the lifetime of the batteries and reducing the costs [1].

As the critical parts in WEH systems, rectifiers function for the radio frequency (RF) to direct current (DC) conversion. Many advanced techniques have been proposed to enhance the fundamental frequency (FF) to DC conversion efficiency [2], [3], [4]. There has been an ongoing effort to achieve multiple frequencies [5], [6], broad bandwidth [7], [8], wide dynamical range [9], and wide load range [10], [11]. Recently, a family of outstanding rectifying metasurfaces was put forward [12], [13]. A solid foundation is laid in the WPT and WEH development by these exceptional investigations.

What can be offered by the rectifying circuit is more than DC. Because the circuit relies on nonlinear interactions between FF signals and nonlinear elements, such as Schottky diodes in most cases, the products also contain harmonic components with the intensities decreasing as the order increases. For the typical rectifying circuits, harmonics are suppressed or recycled. On the other hand, they could be exploited for communications, thus eliminating the need for RF-generating circuits or additional power consumption. This concept is not new. In the field of harmonic radar, harmonics are employed as echo signals from transponders to interrogators. Passive harmonic transponders have been applied in many investigations [14], [15], [16]. Contrary to the rectifiers, harmonic transponders emphasize the SH generation, and DCs are supposed to be blocked.

Recent years have witnessed the exploitation of harmonic components in WPT and WEH in high-power scenarios. Harmonics produced by the rectifiers were employed as the feedback signals to help transmitters collimate narrow beams towards moving rectennas [17], [18], [19], [20], [21]. The harmonic was also employed as the carrier signal for backscattering communications [22], [23]. These studies took advantage of shared hardware for both WEH and wireless communications, providing valuable inspiration for highly integrated self-sustained wireless systems. Since the echo harmonic intensity is strongly associated with the detection accuracy and quality and range of wireless communications, the second harmonic (SH) with the highest intensity among various harmonics is the preferred choice, and enhancing the FF-SH conversion is of great significance. Currently, attempts for simultaneous DC and SH generations are rare, and there is still plenty of room for improving the conversion efficiency. In [20], [22], the SH signals were amplified by using RF amplifiers, which were driven by the DC energy obtained from

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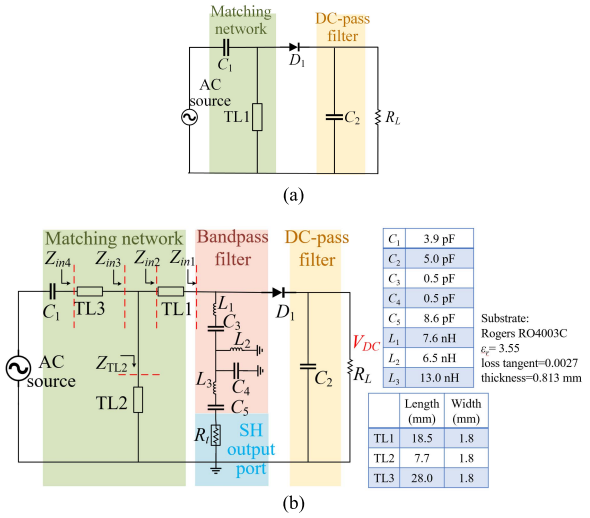

C_1	3.9 pF
C_2	5.0 pF
C_3	0.5 pF
C_4	0.5 pF
C_5	8.6 pF
L_1	7.6 nH
L_2	6.5 nH
L_3	13.0 nH

	Length (mm)	Width (mm)
TL1	18.5	1.8
TL2	7.7	1.8
TL3	28.0	1.8

Fig. 1. (a) Schematic diagram of the traditional single-series diode rectifying circuit. (b) Schematic diagram of the proposed circuit. The values of the lumped components and structural parameters are presented.

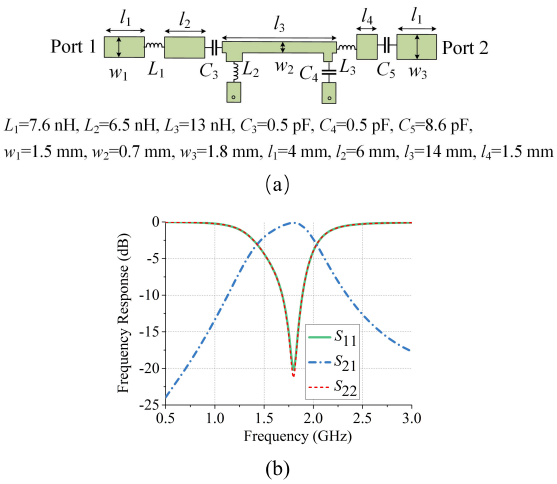

Fig. 2. (a) The proposed bandpass filter functioning as the SH output route, not to scale. (b) Simulated frequency response of the bandpass filter.

the rectifiers. However, the FF-SH efficiency was improved at the expense of an undesired decrease in the FF-DC conversion and overall efficiencies.

In this brief, we propose a novel circuit topology to achieve high-efficiency SH generation while maintaining the typical rectifying function of a conventional circuit. To achieve this, we build a transmitting bandpass route for the SH and connect it to the anode of the Schottky diode, so the SH can be output efficiently without impact on the DC generation. The design is conducted through simulations, fabrications, and measurements. Aiming at dedicated high-power WPT scenarios, the input FF power in this brief is higher than 10 dBm. The FF-SH efficiency reaches up to 12.3% without requiring any amplifiers; in addition, the overall efficiency is 67.3%, which is competitive compared to other ongoing investigations.

II. Circuit Design and Simulations

A. SH Output Design

Fig. 1(a) shows the conventional single-series Schottky diode-based rectifying circuit. It is selected because of its simple configuration, consisting of an alternating-current (AC) source for the FF excitation, an impedance-matching network, a Schottky diode, a capacitor C_2 as the DC-pass filter, and a resistor R_L as the DC load. Based on this, the proposed schematic is displayed in Fig. 1(b). The diode is Schottky diode HSMS-286x from Avago. A bandpass-filter branch terminated by the SH output port is connected to the anode of the diode. The matching network is shown in detail, consisting of a capacitor C_1, two transmission lines TL3 and TL1, and a shunt shorted line TL2. The circuit's operating frequency of 900 MHz is achieved through careful designs of the filter and matching network. This is one of the license-free ISM bands that has been extensively utilized in investigations on WPT [4], [8], [9], [20], [21]. We choose it for developing our WPT and WEH prototype systems.

The SH output path is a bandpass filter connected to the anode of the diode, and it is terminated by an SH output port, whose inner impedance R_t=50 Ω, as shown in Fig. 1(b). Using the classic insertion loss method [24], a three-order filter based on the Butterworth-type one is designed. Its central frequency is 1800 MHz, and the 3-dB bandwidth is from 1.35 to 2.25 GHz. The insertion loss at 900 MHz is larger than 20 dB. After theoretical derivations and optimizations in ADS, its structure is obtained, as shown in Fig. 2(a). The filter exclusively allows the transmission of SH while blocking other frequency components, thereby not interfering with them in the conventional rectifier. At the operational frequency of the filter, i.e., 1800 MHz, its impedance is theoretically zero; thus, the impedance of the filter branch is R_t, which is smaller than that of the AC-source branch. Because the SH output branch and the AC-source branch are connected in parallel, the SH energy reflected by the DC-pass filter is split into two parts and a large portion should be absorbed by R_t, that is, output by the port.

The frequency response of the filter is revealed by simulations in ADS, as shown in Fig. 2(b). The input port is named Port 1, and the output port is named Port 2. This is a reciprocal device. Satisfactory filtering performances can be verified by the reflection and transmission coefficients of the two ports. The reflections at the two ports are below −21 dB at 1800 MHz, and the transmission coefficient here is almost −0.1 dB. The transmission coefficient larger than −3 dB is from 1400 to 2000 MHz. At 900 and 2700 MHz, which are the FF and third harmonic (TH) frequencies, the transmission coefficients are below −15.2 dB.

B. Impedance-Matching Network

The impedance-matching network functions to convert the impedance of the above circuit into 50 Ω, so it can match that of the AC source. The network includes the microstrips TL1, TL2, TL3, and the capacitor C_1.

Through large-signal S-parameter (LSSP) harmonic balance simulations in ADS, the input impedance on the right side of TL1, Z_{in1}, is obtained when the input FF power is 19 dBm and DC load R_L is 300 Ω, as plotted in Fig. 3(a). At 900 MHz, Z_{in1}=(9.5-j49.2) Ω. TL1 and the shunt short-ended line TL2 function to eliminate the imaginary part of Z_{in1}. The input impedance Z_{in2} is theoretically expressed as

$$Z_{in2} = Z_1 \frac{Z_{in1} + jZ_1 \tan\theta_1}{Z_1 + jZ_{in1} \tan\theta_1}, \quad (1)$$

where Z_1 and θ_1 are the characteristic impedance and electric length of TL1 at 900 MHz, respectively. The input impedance Z_{in3} on the right side of TL3 satisfies

$$\frac{1}{Z_{in3}} = \frac{1}{Z_{in2}} + \frac{1}{Z_{TL2}}. \tag{2}$$

$Z_{TL2} = jZ_2 \tan\theta_2$ is the input impedance of shunt shorted TL2, where Z_2 and θ_2 are its characteristic impedance and electric length at 900 MHz, respectively. For simplicity, Z_1 and Z_2 are set to be 50 Ω, and their lengths are carefully chosen. Moreover, because the filter branch is folded for compactness, a small length is chosen for TL2. The electric lengths of TL1 and TL2 are 33° and 14°, corresponding to 18.5 and 7.7 mm, respectively. Fig. 3(a) plots the input impedances Z_{in2} and Z_{in3}, showing that the imaginary part is getting close to zero. At 900 MHz, Z_{in3}=(21.3+j0.93) Ω.

Theoretically, a 1/4-wavelength transmission line could be the first choice for TL3 to convert the real part of Z_{in3} to 50 Ω. Here, we try to reduce the length as much as possible. Supposing that the characteristic impedance and electric length of TL3 are Z_3 and θ_3, respectively, we have

$$\begin{aligned} Z_{in4} &= Z_3 \frac{Z_{in3} + jZ_3 \tan\theta_3}{Z_3 + jZ_{in3} \tan\theta_3} \\ &= Z_3 \frac{\left(1+\tan^2\theta_3\right) Z_3 Z_{in3} + j \tan\theta_3 \left(Z_3{}^2 - Z_{in3}{}^2\right)}{Z_3{}^2 + Z_{in3}{}^2 \tan^2\theta_3}. \end{aligned} \tag{3}$$

The real part of Z_{in4} should be matched to R_0, which is the impedance of the AC source. So,

$$Z_3 \frac{\left(1+\tan^2\theta_3\right) Z_3 Z_{in3}}{Z_3{}^2 + Z_{in3}{}^2 \tan^2\theta_3} = R_0, \tag{4}$$

which can be written as

$$\tan^2\theta_3 = \frac{R_0 - Z_{in3}}{Z_{in3}} \frac{1}{1 - R_0 Z_{in3}/Z_3{}^2}. \tag{5}$$

Because R_0=50 Ω and Z_{in3} is almost 21.3 Ω, (5) can be approximately transformed into

$$\tan^2\theta_3 = 1.5 \cdot \frac{1}{1 - 1000/Z_3{}^2}. \tag{6}$$

Since $\tan^2\theta_3 \geq 0$ in (6), Z_3 should not be smaller than 31.6 Ω. Z_3=31.6 Ω is exactly the case of the 1/4-wavelength impedance matching. If Z_3 is infinite, θ_3 has the smallest value of 50.2°, corresponding to 27.9 mm at 900 MHz. In other words, the theoretical range of TL3's length is between 27.9 to 51 mm. In this brief, the characteristic impedance of 50 Ω is chosen for TL3, and its final length is 28 mm after optimizations. The simulated Z_{in4} is illustrated in Fig. 3(a) with the real part of 50.3 Ω and the imaginary part of j42.5 Ω at 900 MHz. Finally, the input impedance is transformed to 50 Ω through C_1 of 3.9 pF.

Fig. 3(b) presents the input reflection coefficients of the circuit with various input power levels after the impedance-matching. The curves are stable when the power changes from 12 to 19 dBm, and the values are below −10 dB in the frequency range from 860 to 930 MHz. As the power reaches 22 dBm, the bandwidth moves slightly downwards. Here the impedance-matching bandwidth is narrow due to the simple matching network; a wider bandwidth could be potentially achieved by advanced techniques, a coupled line for example [8].

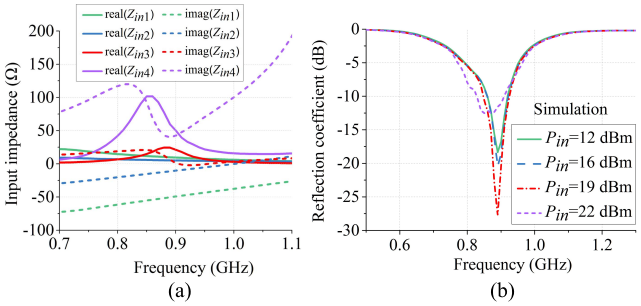

Fig. 3. (a) Simulated results of the input impedance Z_{in1} through Z_{in4}. (b) Simulated input reflection coefficients of the circuit with varying input FF power levels.

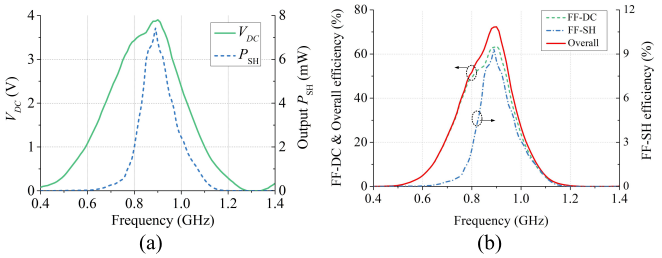

Fig. 4. Simulated performances of the circuit when the input FF power is 19 dBm and the DC load is 300 Ω. (a) DC voltage across the load and the generated SH power. (b) FF-DC, FF-SH, and overall conversion efficiencies.

C. Simulated Nonlinear Properties

The FF-DC and FF-SH performances of the circuit are analyzed through the simulations. The SH power can be directly obtained from its port, and the DC power can be calculated by monitoring the voltage across the load V_{DC}. The conversion efficiencies can be calculated using (7) and (8), respectively.

$$\eta_{\text{FF-DC}} = \frac{P_{\text{DC}}}{P_{\text{FF}}} \times 100\% = \frac{V_{\text{DC}}{}^2}{R_L} \times \frac{1}{P_{\text{FF}}} \times 100\%, \tag{7}$$

$$\eta_{\text{FF-SH}} = \frac{P_{\text{SH}}}{P_{\text{FF}}} \times 100\%. \tag{8}$$

The overall conversion efficiency is thus given by $\eta = \eta_{\text{FF-DC}} + \eta_{\text{FF-SH}}$. Here P_{FF}= 19 dBm and R_L = 300 Ω. Fig. 4(a) presents the DC voltage and SH power versus frequency, and Fig. 4(b) plots the FF-DC, FF-SH, and overall conversion efficiencies.

The best performances are achieved around 900 MHz. The DC voltage reaches the largest value of 3.9 V at 900 MHz, corresponding to the highest FF-DC conversion efficiency of 63.8%. At this frequency, the SH power is 6.8 mW, and thus the FF-SH conversion efficiency is 8.6%. The overall conversion efficiency at 900 MHz is 72.4%. The largest SH power occurs when the FF is 890 MHz. The value is 7.4 mW, corresponding to the highest FF-SH efficiency of 9.4%. At this frequency, the DC voltage is almost 3.87 V, so the FF-DC efficiency is 62.9%. The overall conversion efficiency is 72.3%. We also check the TH power, which is 0.02 mW, corresponding to an FF-TH conversion efficiency of 0.028%. Intensities of higher harmonics are even lower, so they are ignored.

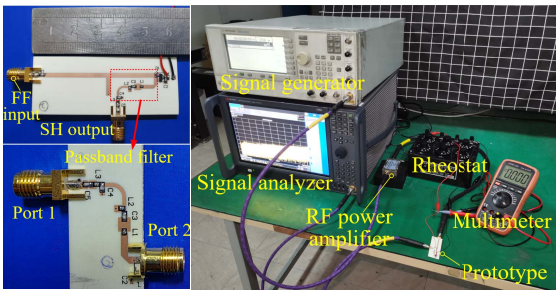

Fig. 5. Photographs of (a) the circuit and the bandpass filter and (b) the experimental setup for the efficiency measurement.

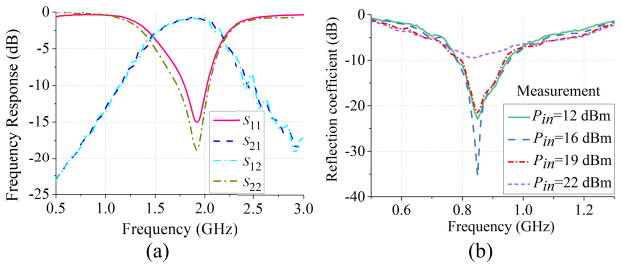

Fig. 6. (a) Measured frequency response of the bandpass filter. (b) Measured input reflection coefficients of the circuit with varying input power levels.

III. Measurements and Discussions

The bandpass filter and the circuit are fabricated and measured. The SH output branch is folded for compactness. As shown in Fig. 5(a), the circuit board measures 61 mm × 24 mm ($0.3\lambda_g \times 0.12\lambda_g$), where λ_g is the guided wavelength at 900 MHz.

The bandpass filter is measured using a vector network analyzer (VNA) (Agilent N5230C). Port 1 is the one that should output the SH, and Port 2 is supposed to be connected to the rectifying circuit. The results given in Fig. 6(a) are in good accord with the simulation. The reflection coefficients at Port 2 are −0.22 dB at 900 MHz and −0.75 dB at 2700 MHz, indicating that these frequencies are strongly blocked. At 1800 MHz, the transmission coefficient from Port 2 to 1 is −0.94 dB. Then, the reflection coefficient at the input port of the rectifying circuit is measured. The port is connected to the VNA, and the SH output port is connected to a 50-Ω load. The DC load is 300 Ω. Fig. 6(b) presents the results with various input power levels, which agree well with the simulations. The values are below −10 dB from 800 to 940 MHz, showing a good impedance-matching property.

Fig. 5 shows the photograph of the experimental setup for the rectification and SH-output performances. The output of a signal generator (Agilent E8257D) is connected to the input port of an RF power amplifier with a gain of 27 dB. Before the measurement, the power from the amplifier is calibrated by connecting its output port to a signal analyzer (Keysight N9040B) through a 30-dB attenuator. After that, the input port of the prototype is connected to the amplifier, and its SH output port is connected to the signal analyzer. A rheostat serves as the load resistor. The DC voltage across the load is monitored by a multimeter. The insertion loss of the coaxial lines is 0.5 dB.

The nonlinear measurements are firstly carried out with the fixed R_L of 300 Ω. Fig. 7(a)(c)(e) presents the results when the input FF power level P_{in} varies from 10 to 19 dBm.

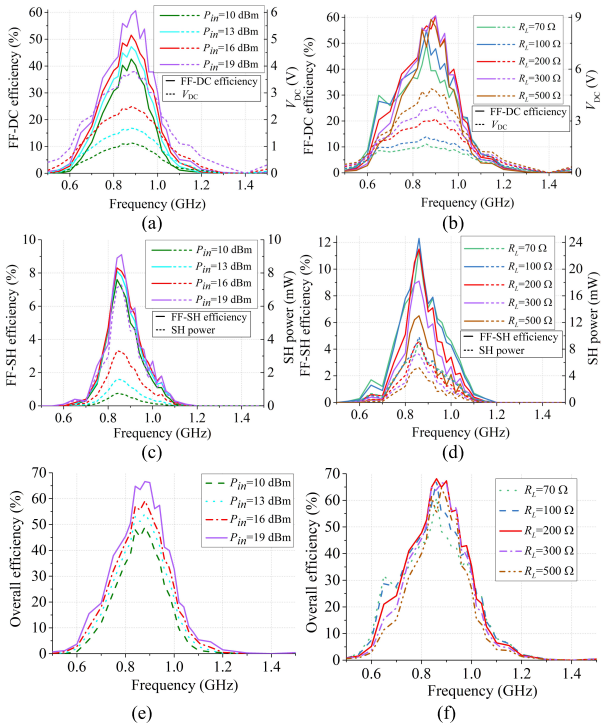

Fig. 7. (a)(c)(e) Measured results with R_L =300 Ω and varying input FF power levels. (b)(d)(f) Measured results with the input power of 19 dBm and varying R_L. (a)(b) Output DC voltage and FF-DC efficiency. (c)(d) Output SH power and FF-SH efficiency. (e)(f) Overall efficiency.

Fig. 7(a) provides the output DC voltages V_{DC} across the load and the calculated $\eta_{\text{FF-DC}}$, showing their enhancement by increasing the FF power. Fig. 7(c) plots the output SH power and the $\eta_{\text{FF-SH}}$, which are also enhanced by the input power. The maximum DC voltage of 3.8 V is achieved at 900 MHz ($\eta_{\text{FF-DC}}$=60.6%). The SH power at this frequency is 4.5 mW ($\eta_{\text{FF-SH}}$ =5.6%). At 860 MHz, the SH power reaches the maximum level of 7.3 mW ($\eta_{\text{FF-SH}}$= 9.1%); the DC voltage is 3.6 V ($\eta_{\text{FF-DC}}$= 54.4%). The overall efficiencies are given in Fig. 7(e), showing that around 65% is achieved from 840 to 900 MHz when P_{in} = 19 dBm. The maximum overall efficiency of 66.6% occurs at 880 MHz, which is composed of $\eta_{\text{FF-DC}}$ of 59.0% and $\eta_{\text{FF-SH}}$ of 7.6%.

Then, the circuit is measured by keeping P_{in} = 19 dBm and varying R_L from 70 to 500 Ω. The results are presented in Fig. 7(b)(d)(f). Fig. 7(b) shows that V_{DC} is enhanced by increasing R_L, but $\eta_{\text{FF-DC}}$ remains almost stable when R_L ≥ 200 Ω. At 900 MHz, $\eta_{\text{FF-DC}}$ reaches the largest value of 60.6% (V_{DC}=3.8 V) when R_L= 300 Ω. The results of the SH generation are shown in Fig. 7(d). They are strongly affected by R_L and are better at 860 MHz than those at other frequencies. The best result is achieved when R_L =100 Ω. At 860 MHz, the SH power reaches the highest value of 9.8 mW, corresponding to the largest $\eta_{\text{FF-SH}}$ of 12.3%. As R_L increases, the efficiency drops accordingly. Fig. 7(f) offers the overall efficiencies as R_L changes.

Observing Fig. 7(b) and (d), two important results should be remarked. First, the highest overall efficiency of 68.1% is achieved at 860 MHz with R_L=200 Ω ($\eta_{\text{FF-DC}}$= 56.7% and $\eta_{\text{FF-SH}}$=11.5%). Secondly, when R_L= 100 Ω, the highest $\eta_{\text{FF-SH}}$ of 12.3% is reached at 860 MHz; $\eta_{\text{FF-DC}}$= 55.0%, and the overall efficiency is 67.3%. Compared with the simulations, the best frequency moves downwards slightly by

TABLE I
COMPARISON BETWEEN THIS BRIEF AND THE STATE-OF-THE-ART RECTIFYING CIRCUITS WITH SIMULTANEOUS SH AND DC GENERATIONS

Ref.	FF (GHz)	R_L (Ω)	P_{in} (dBm)	$\eta_{FF\text{-}SH}$	$\eta_{FF\text{-}DC}$	Overall eff.
[21]	0.915	1k	BC 15	2.0%	67.0%	69.0%
[22]	0.4645	1k	BC 19	3.8% 14.8% [a]	61.0% 33.0%	64.8% 47.8%
[23]	2.4	9k	BC 4	7.1%	60.0%	67.1%
This work	**0.9**	**100**	**BC 19**	**12.3%**	**55.0%**	**67.3%**

[a] The generated SH was amplified by an amplifier, which is driven by the DC generated by the rectifier. FF=fundamental frequency. BC=best case.

40 MHz, which can be attributed to fabrication and soldering errors.

Analyzing the distribution of system efficiency, consider the case with R_L=100 Ω and P_{in}= 19 dBm. At 860 MHz, the return loss is 20.3 dB, implying a mismatch loss of 1%. The substrate loss accounts for the efficiency reduction of 5% [4]. Based on the SH power and the filter's transmission coefficient, the filter results in a 3.5% decrease in the system efficiency. Considering $\eta_{FF\text{-}SH}$=12.3% and $\eta_{FF\text{-}DC}$= 55.0%, the diode loss is estimated to be 23.2%. The filter results in a distinctive SH generation with an almost ignorable impact on the rectifying function of the circuit; thus, a relatively high overall efficiency is achieved.

Table I compares the state-of-the-art works for simultaneous generations of SH and DC. Ref. [21], [22] and our work are designed for high-power conditions. Although an SH efficiency of up to 14.8% was reported [22], it was obtained by using an amplifier driven by the harvested DC energy. Our work achieves the highest $\eta_{FF\text{-}SH}$ of 12.3% without an amplifier. While the reduction of $\eta_{FF\text{-}DC}$ does come at a cost, the overall efficiency remains competitive with others. Specifically, our overall efficiency is only 1.7% lower than that of [21], but $\eta_{FF\text{-}SH}$ is higher by 10.3%. In our future work, we aim to simplify the SH route and mitigate its loss. This could be achieved by reducing the number of components or selecting components with lower loss.

IV. CONCLUSION

In summary, a rectifying circuit is proposed with the high-performance SH and DC generations. The key is the introduction of a bandpass filter that re-arranges the SH power flow without impact on DC. The circuit is fabricated and studied experimentally. When the input FF power is 19 dBm, the circuit offers an SH power of 9.8 mW, corresponding to an FF-SH conversion efficiency of 12.3%; at the same time, the FF-DC conversion efficiency is 55.0%, giving rise to an overall conversion efficiency of 67.3%. The proposal can be potentially useful in WPT, WEH, and self-sustained backscattering applications.

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